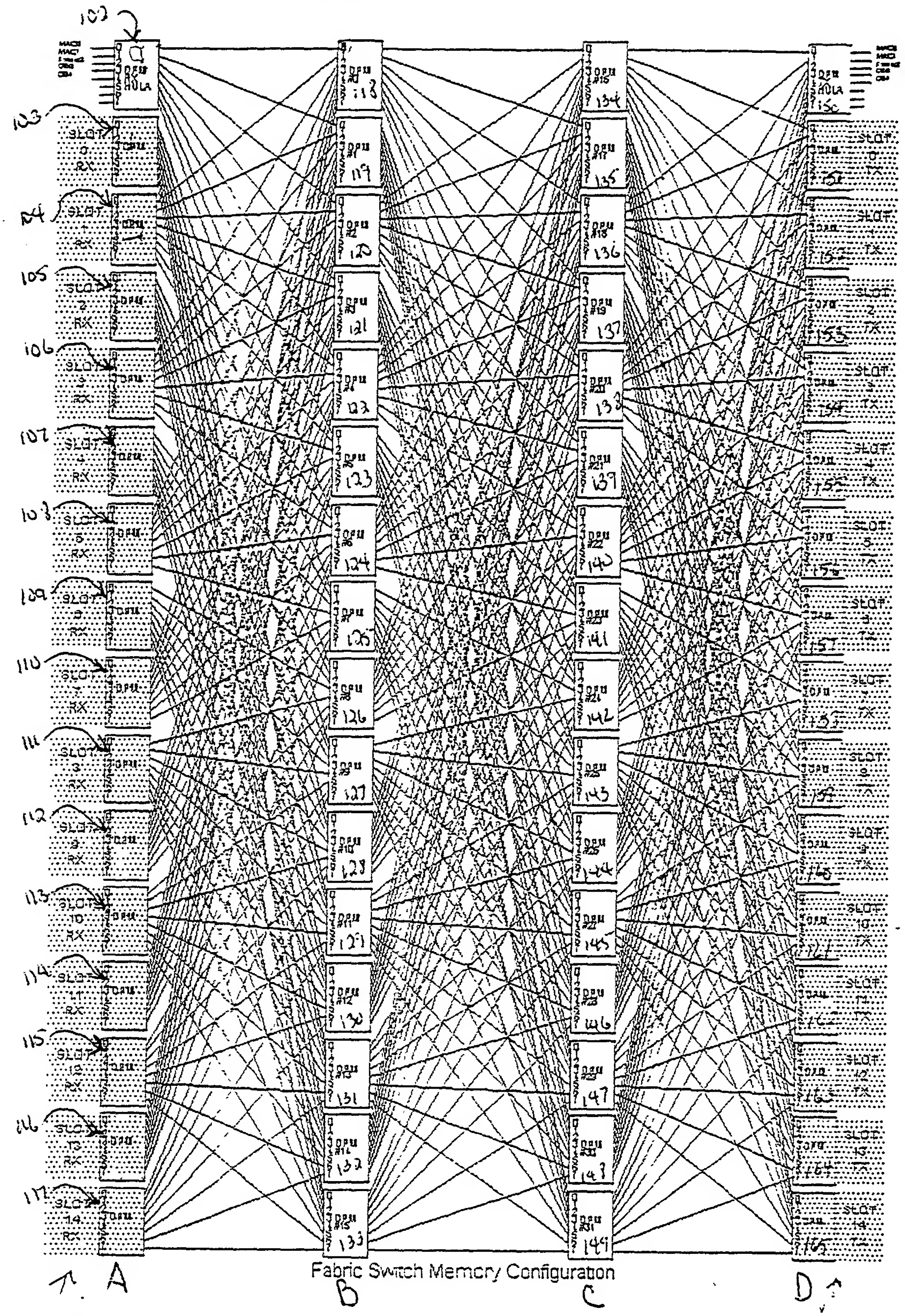
F re lieq

CONFIDENTIAL



Fabric Switch Memory Configuration

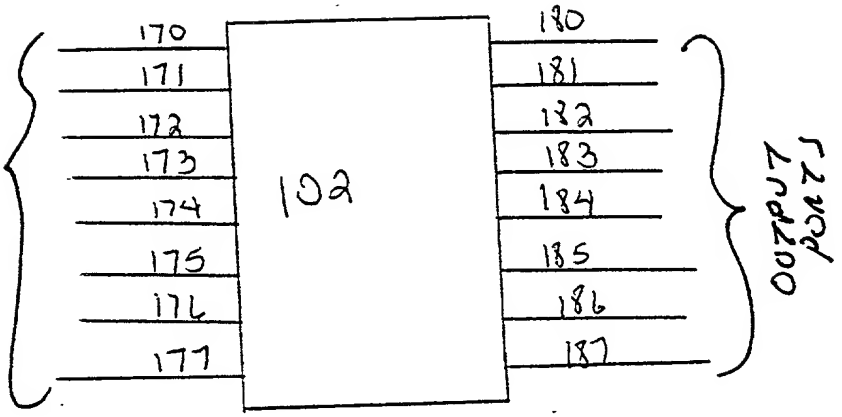

170
171
172
173
174
175
176
177
102
180
181
182
183
184
185
186
187
Output Port

Figure 1b

Figure 1c

Port 1	Port 2	Port 3	Port 4	Port 5	Port 6	Port 7	Port 8
1	1	1	1	1	1	1	1
2	2	2	2	2	2	2	2
3	3	3	3	3	3	3	3
4	4	4	4	4	4	4	4
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
1024	1024	1024	1024	1024	1024	1024	1024

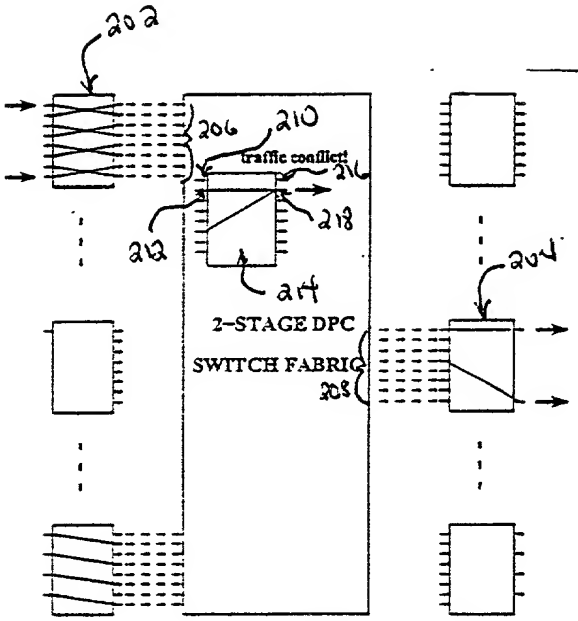


Figure 2

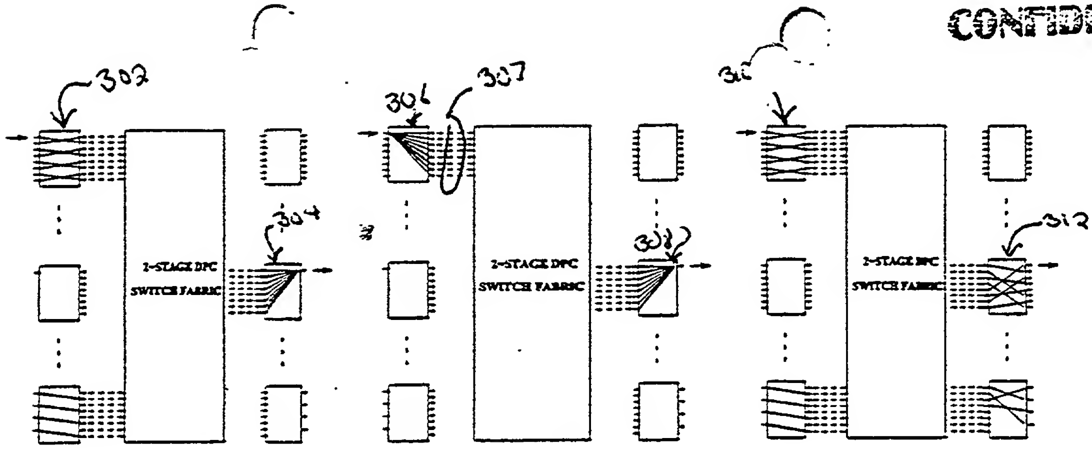


Figure 3

Figure 4

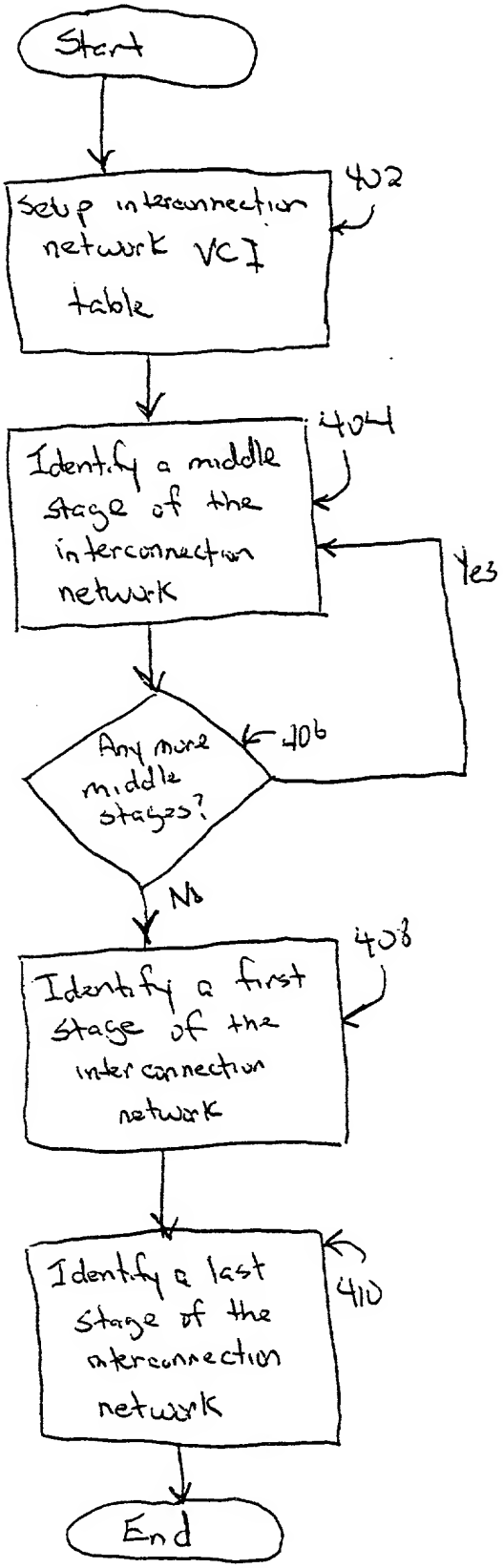

Start
Setup interconnection network VCI table
402
Identify a middle stage of the interconnection network
404
Yes
Any more middle stages?
406
No
Identify a first stage of the interconnection network
408
Identify a last stage of the interconnection network
410
End

Figure 5

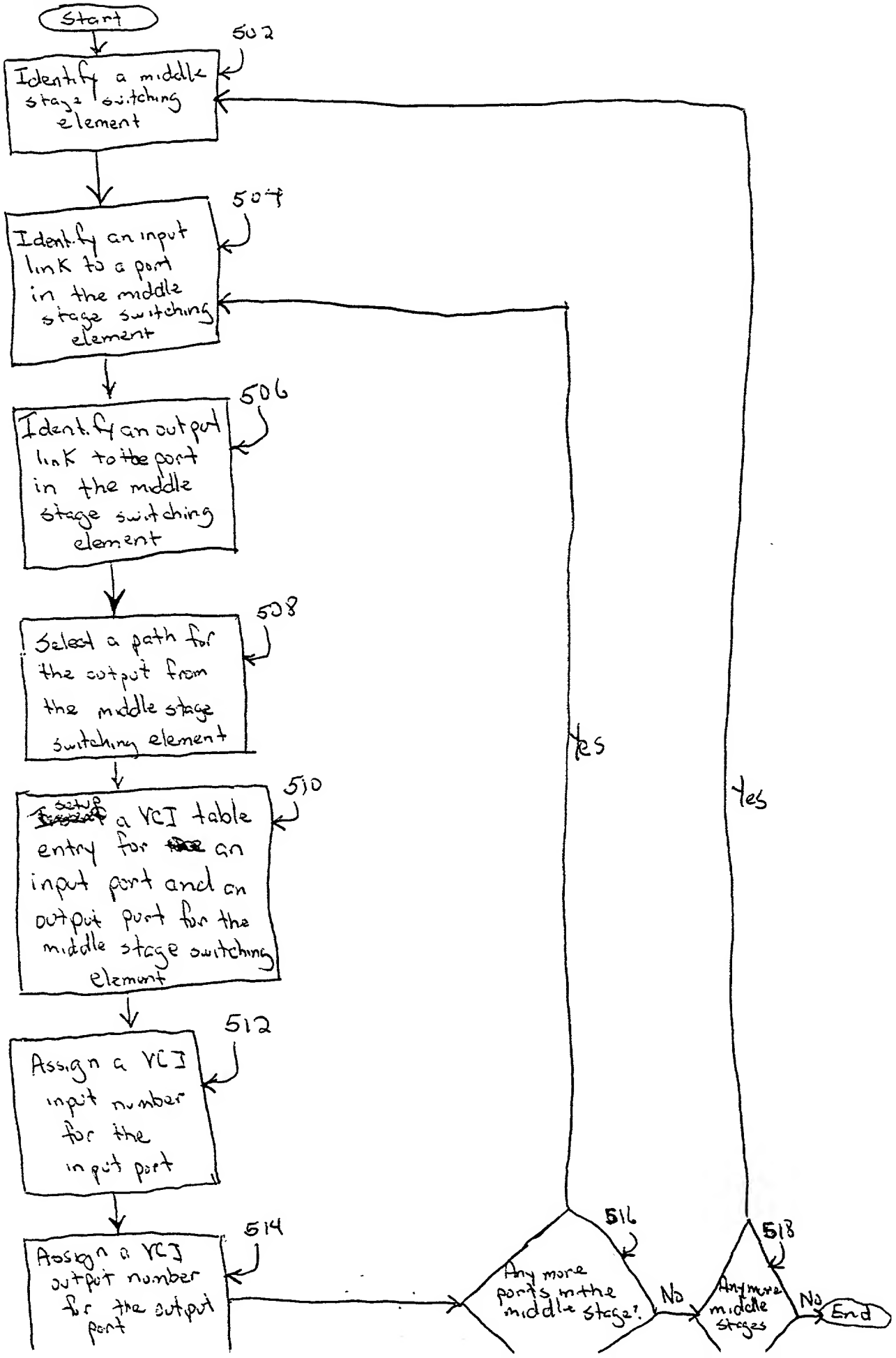

Start
502
Identify a middle stage switching element
504
Identify an input link to a port in the middle stage switching element
506
Identify an output link to the port in the middle stage switching element
508
Select a path for the output from the middle stage switching element
510
Setup a VCI table entry for an input port and an output port for the middle stage switching element
512
Assign a VCI input number for the input port
514
Assign a VCI output number for the output port
516
Any more ports in the middle stage?
Yes
No
518
Any more middle stages
Yes
No
End

Figure 6

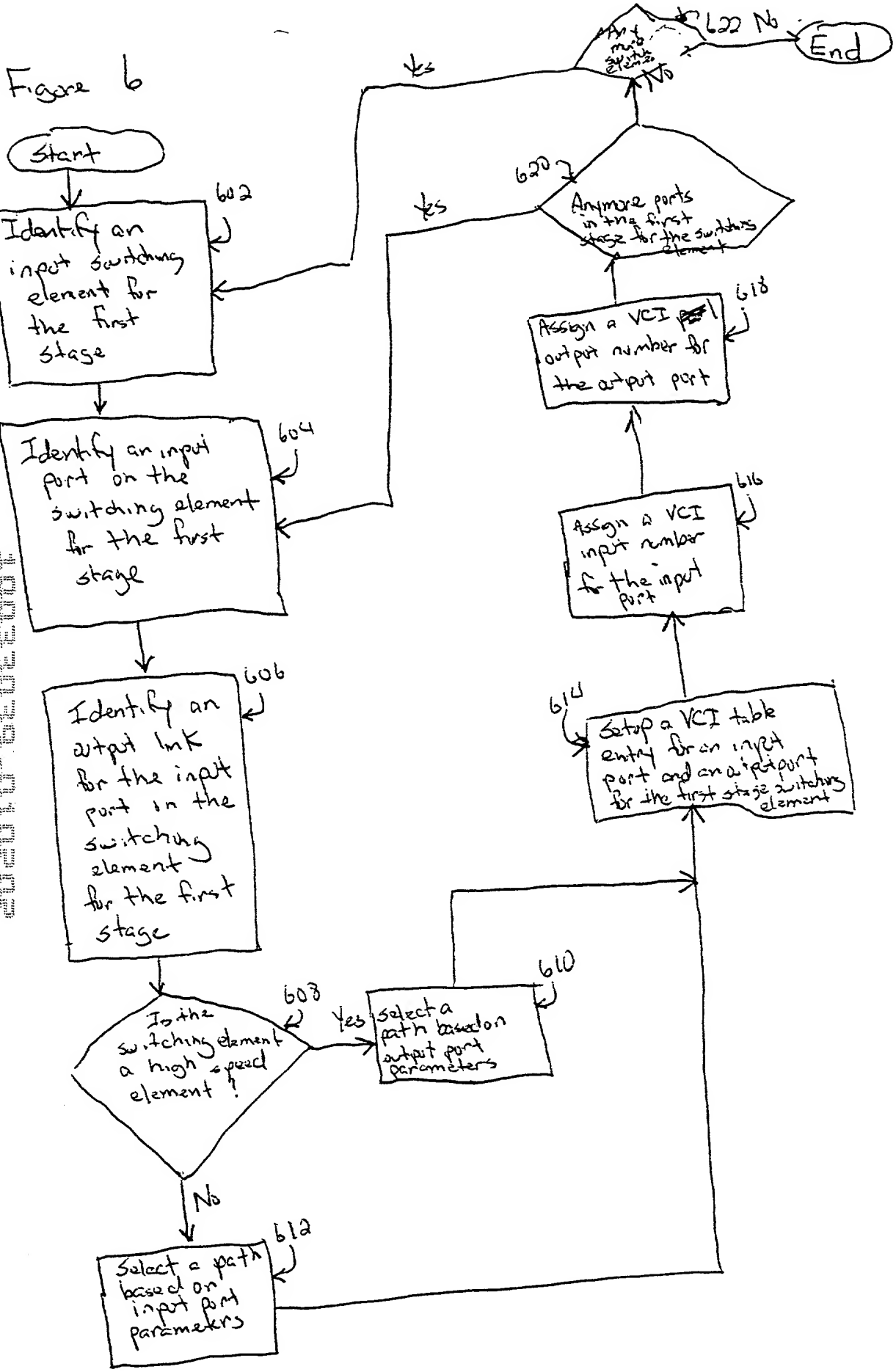

Start
Identify an input switching element for the first stage
602
Identify an input port on the switching element for the first stage
604
Identify an output link for the input port in the switching element for the first stage
606
Is the switching element a high speed element ?
608
Yes
Select a path based on output port parameters
610
No
Select a path based on input port parameters
612
Setup a VCI table entry for an input port and an output port for the first stage switching element
614
Assign a VCI input number for the input port
616
Assign a VCI output number for the output port
618
Anymore ports in the first stage for the switching element
620
Yes
Any more switching elements
622
No
End

Figure 7

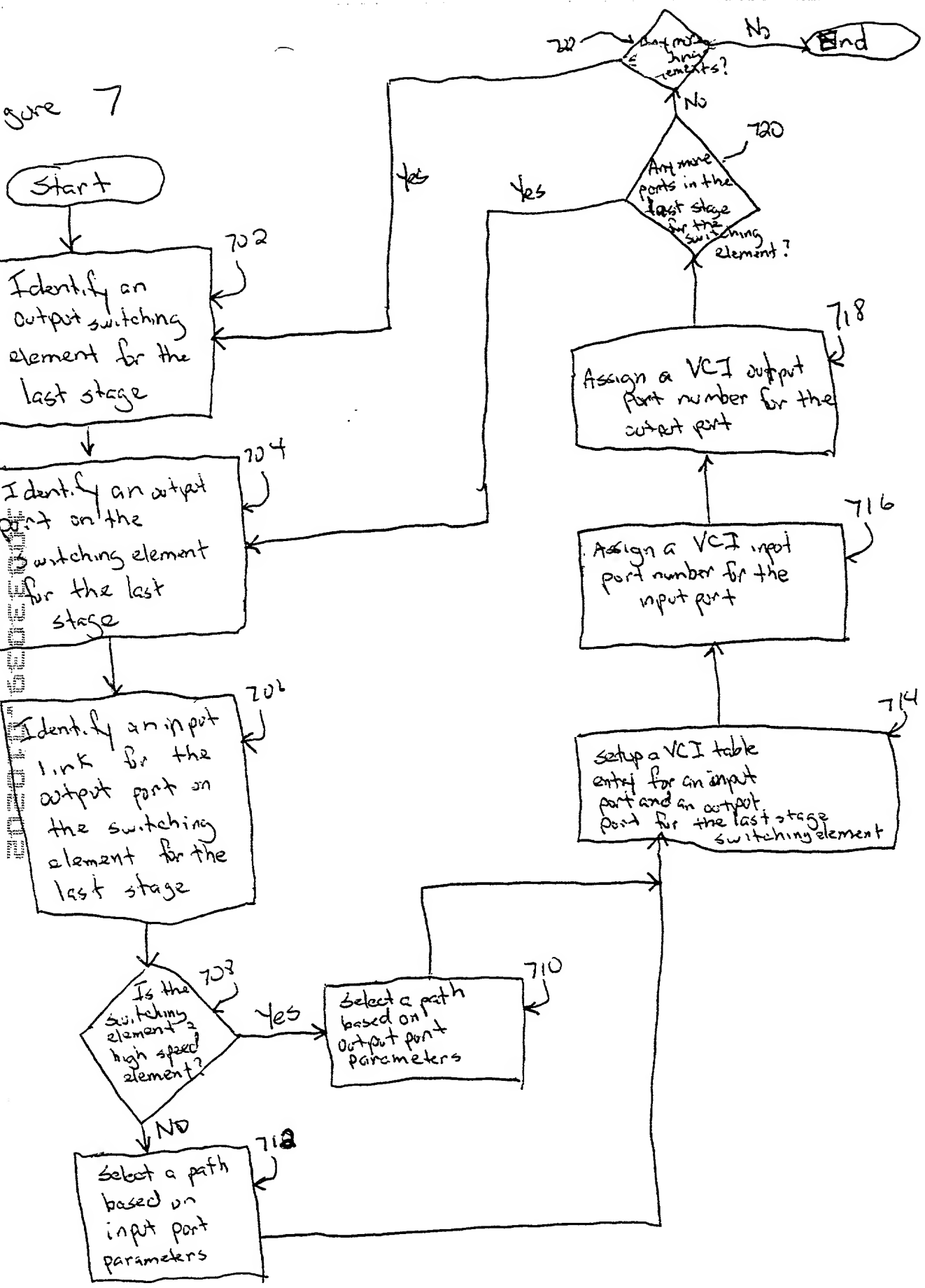

Start
Identify an output switching element for the last stage
702
Identify an output port on the switching element for the last stage
704
Identify an input link for the output port on the switching element for the last stage
706
Is the switching element a high speed element?
708
Yes
No
Select a path based on output port parameters
710
Select a path based on input port parameters
712
Setup a VCI table entry for an input port and an output port for the last stage switching element
714
Assign a VCI input port number for the input port
716
Assign a VCI output port number for the output port
718
Any more ports in the last stage for the switching element?
720
Yes
Any more switching elements?
722
No
End

Figure 8

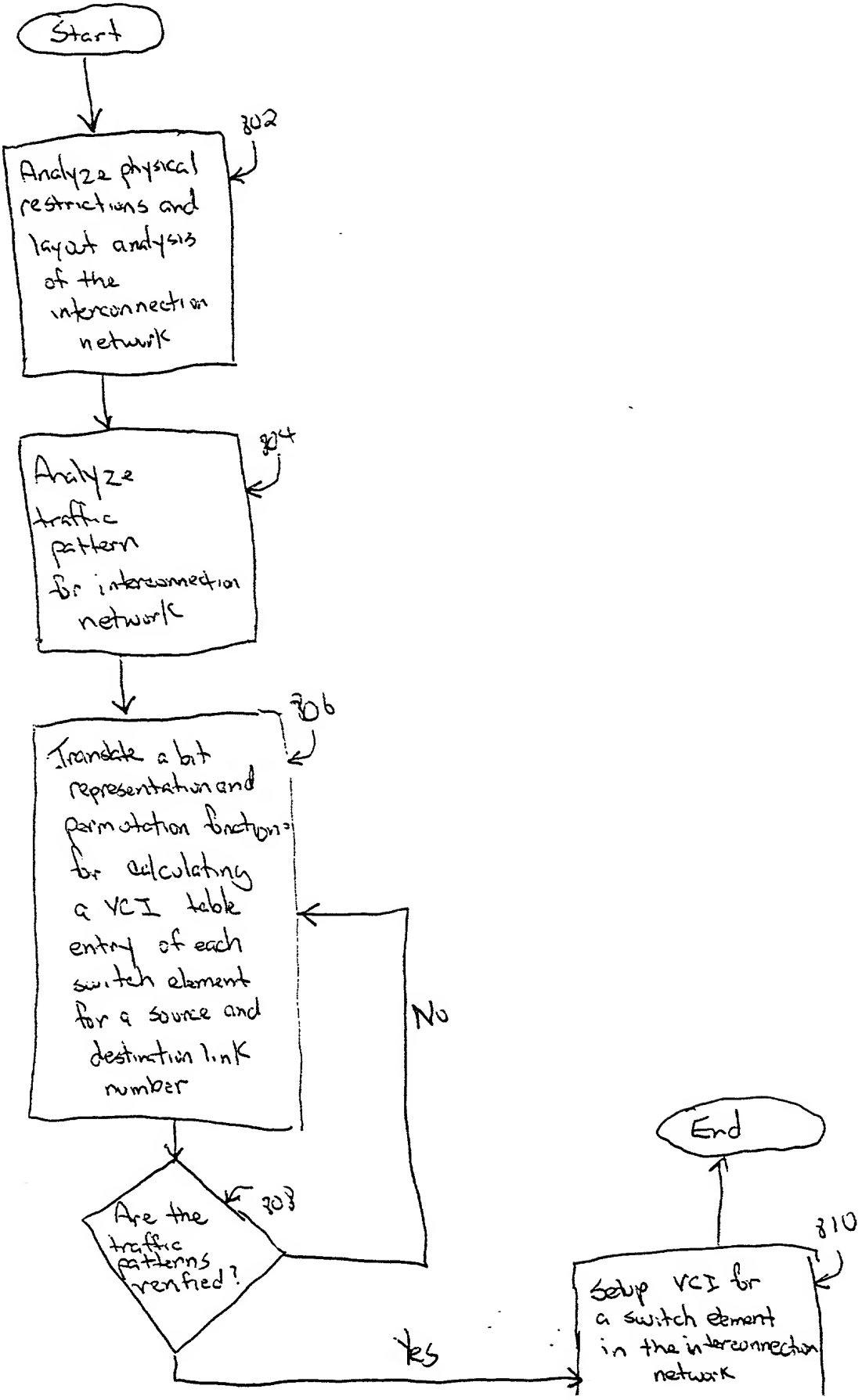
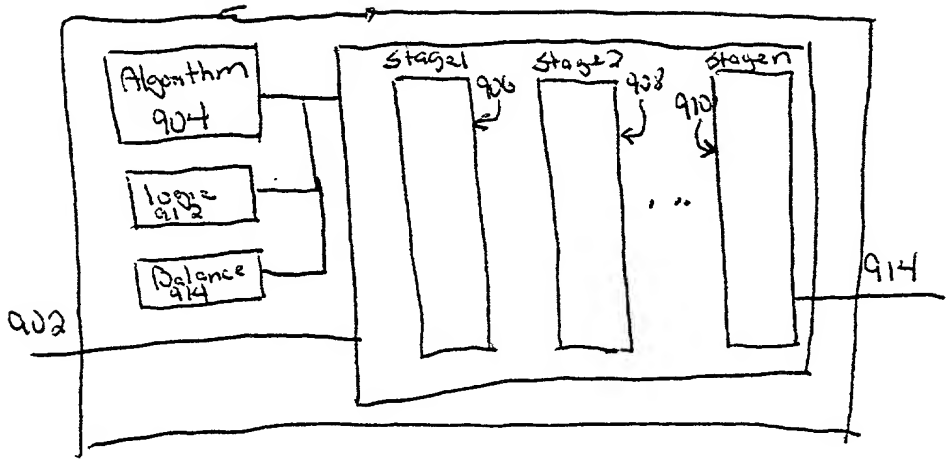

Start
802
Analyze physical restrictions and layout analysis of the interconnection network
804
Analyze traffic pattern for interconnection network
806
Translate a bit representation and permutation function for calculating a VCI table entry of each switch element for a source and destination link number
808
Are the traffic patterns verified?
No
Yes
810
Setup VCI for a switch element in the interconnection network
End

Figure 9


Algorithm
904
Logic
912
Distance
914
902
Stage1
Stage2
Stagen
916
918
910
914

STATGE[0] :: fs

input = (i[6],i[5],i[4],i[3]): (i[2],i[1],i[0]) – (j[6],j[5],j[4],j[3],j[2],j[1],j[0])

output = (i[6],i[5],i[4],i[3]):

STATGE[1] :: ms1

input =

output =

STATGE[2] :: ms2

input =

output =

STATGE[3] :: ls

input = (j[6],j[5],j[4],j[3]):

output = (j[6],j[5],j[4],j[3]): (j[2],j[1],j[0]) – (i[6],i[5],i[4],i[3],i[2],i[1],i[0])

10 (a) Initial step 0

STATGE[0] :: fs

input = (i[6],i[5],i[4],i[3]): (i[2],i[1],i[0]) – (j[6],j[5],j[4],j[3],j[2],j[1],j[0])

output = (i[6],i[5],i[4],i[3]):

STATGE[1] :: ms1

input = (i[3], a , b , c) : (i[6],i[5],i[4]) –

output = (i[3], a , b , c) :

STATGE[2] :: ms2

input = (c , d , e ,j[6]) : (i[3], a , b) –

output = (c , d , e ,j[6]) :

STATGE[3] :: ls

input = (j[6],j[5],j[4],j[3]): (c , d , e) –

output = (j[6],j[5],j[4],j[3]): (j[2],j[1],j[0]) – (i[6],i[5],i[4],i[3],i[2],i[1],i[0])

10(b) Step 1

STATGE[0] :: fs

input = (i[6],i[5],i[4],i[3]): (i[2],i[1],i[0]) – (j[6],j[5],j[4],j[3],j[2],j[1],j[0])

output = (i[6],i[5],i[4],i[3]): (a , b , c) –

STATGE[1] :: ms1

input = (i[3], a , b , c) : (i[6],i[5],i[4]) –

output = (i[3], a , b , c) : (d , e ,j[6]) –

STATGE[2] :: ms2

input = (c , d , e ,j[6]) : (i[3], a , b) –

output = (c , d , e ,j[6]) : (j[5],j[4],j[3])–

STATGE[3] :: ls

input = (j[6],j[5],j[4],j[3]): (c , d , e) –

output = (j[6],j[5],j[4],j[3]): (j[2],j[1],j[0]) – (i[6],i[5],i[4],i[3],i[2],i[1],i[0])

10 (c) Step 2

STATGE[0] :: fs

input = (i[6],i[5],i[4],i[3]): (i[2],i[1],i[0]) – (j[6],j[5],j[4],j[3],j[2],j[1],j[0])

output = (i[6],i[5],i[4],i[3]): (a , b , c) –

STATGE[1] :: ms1

input = (i[3], a , b , c) : (i[6],i[5],i[4]) –

output = (i[3], a , b , c) : (d , e ,j[6]) –

STATGE[2] :: ms2

input = (c , d , e ,j[6]) : (i[3], a , b) –

output = (c , d , e ,j[6]) : (j[5],j[4],j[3])–

STATGE[3] :: ls

input = (j[6],j[5],j[4],j[3]): (c , d , e) –

output = (j[6],j[5],j[4],j[3]): (j[2],j[1],j[0]) – (i[6],i[5],i[4],i[3],i[2],i[1],i[0])

10 (d) Physical restriction bit assignment

FIG. 10

50001.2103

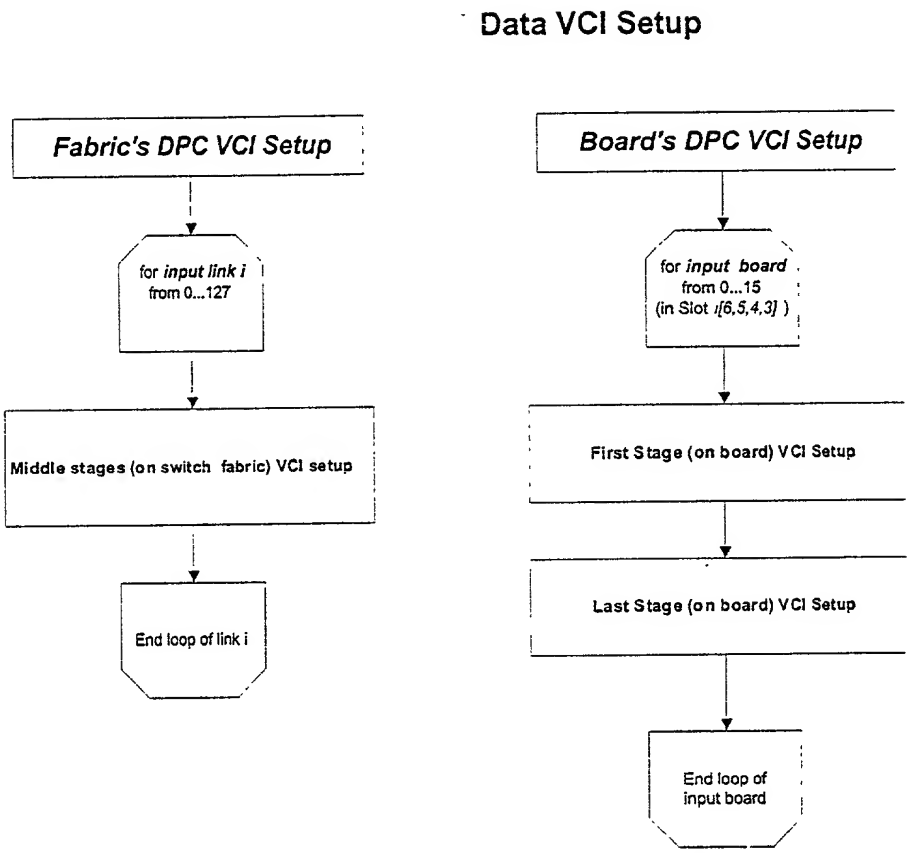


FIG. 11

50001. 2103

Middle Stages (on switch fabric) VCI Setup

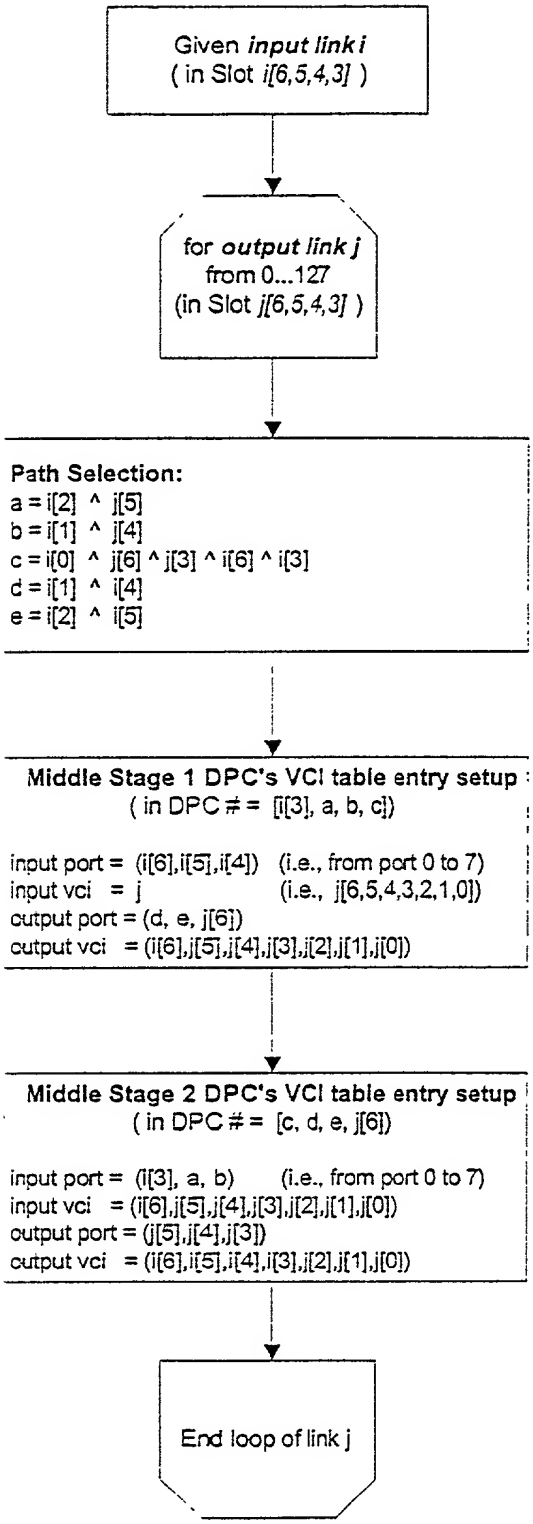


FIG. 12

Data VCI setup within the fabric (for middle stage DPCs)

5000/. 2103

First Stage (on board) VCI Setup

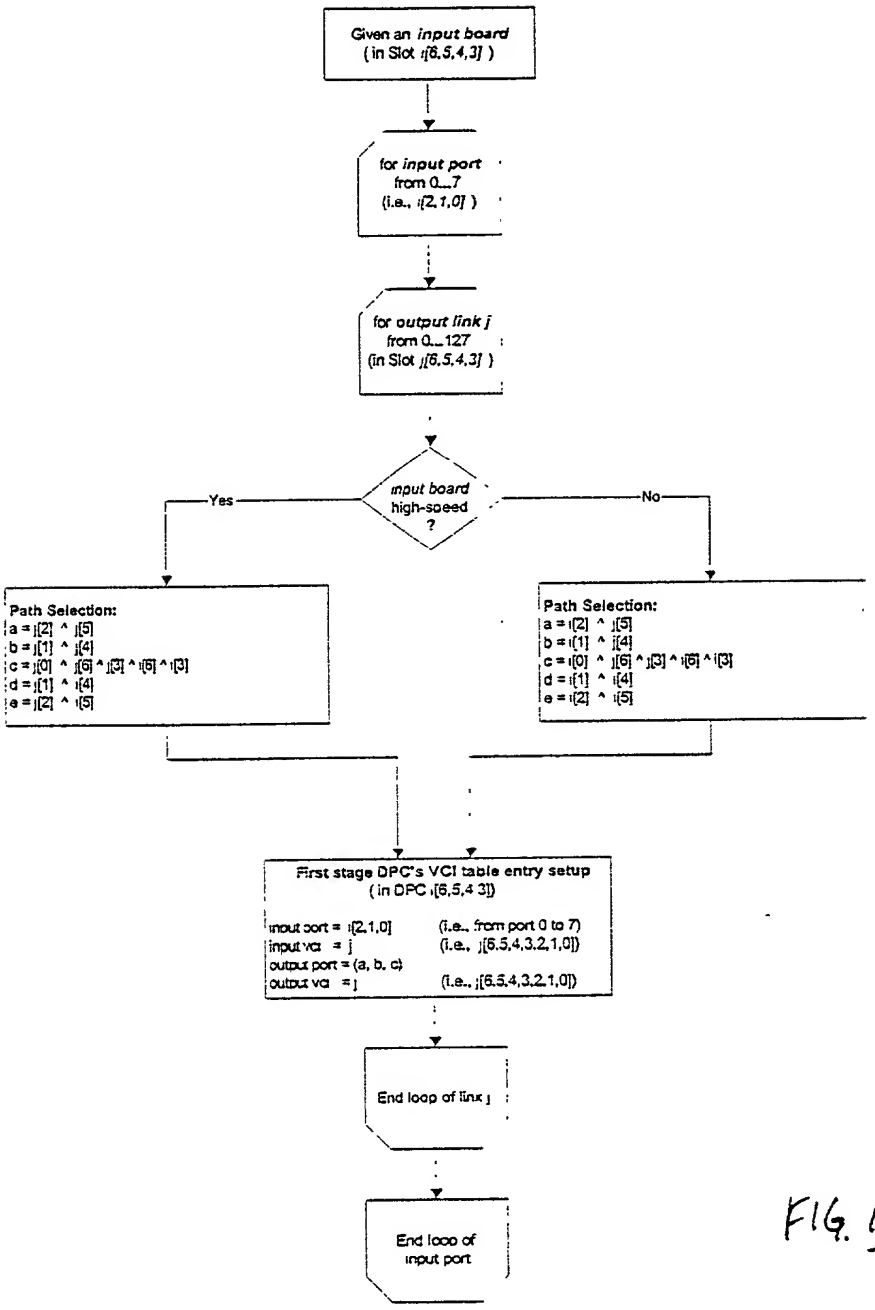


FIG. 13

First stage VCI setup on the board

50001. 2103

Last Stage (on boa rd) VCI Setup

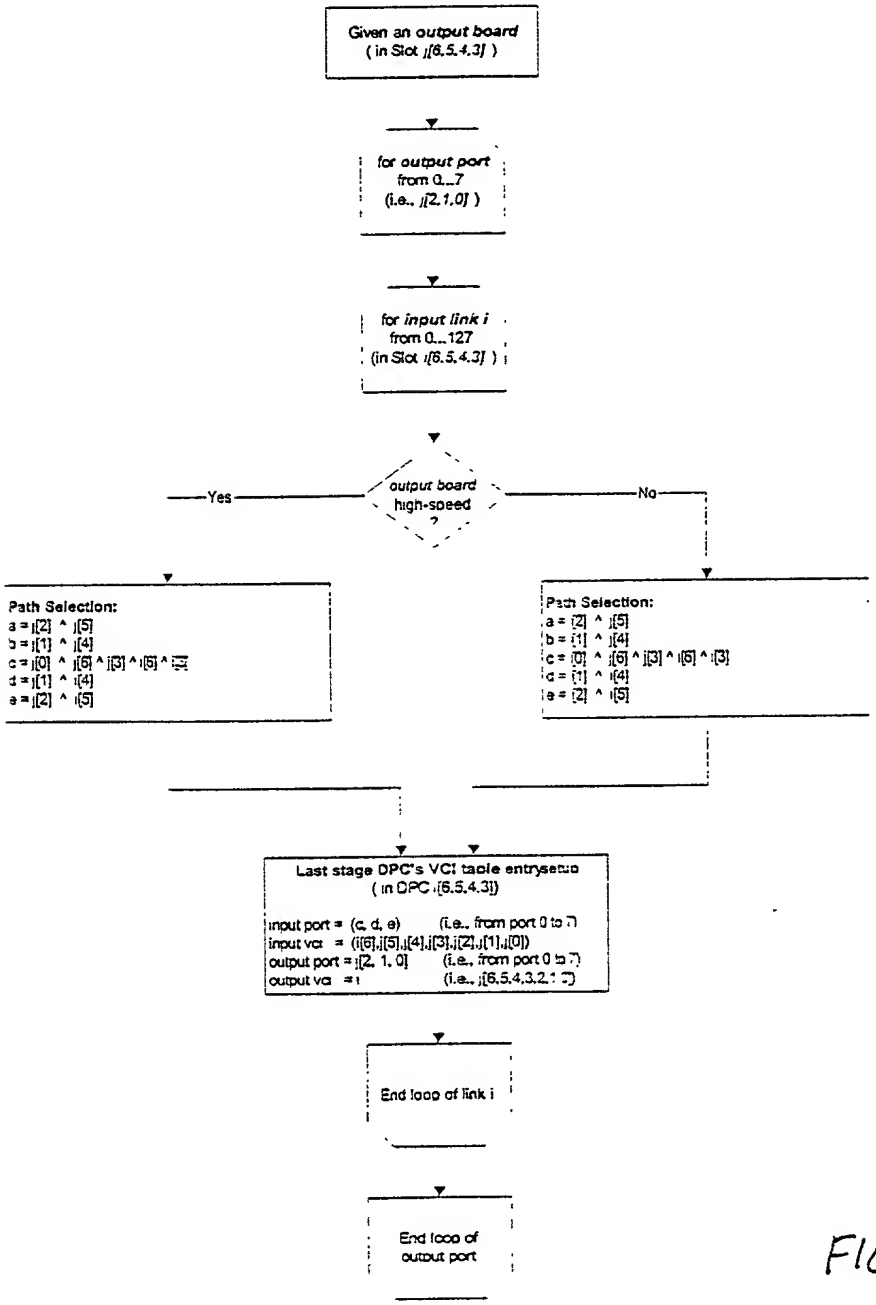


FIG. 14

Last stage VCI setup on the board